



# A wearable intelligent system for the health of expectant mom's and their children

G. Danese, F. Leporati, A. Majani, G. Matrone, E. Merlino



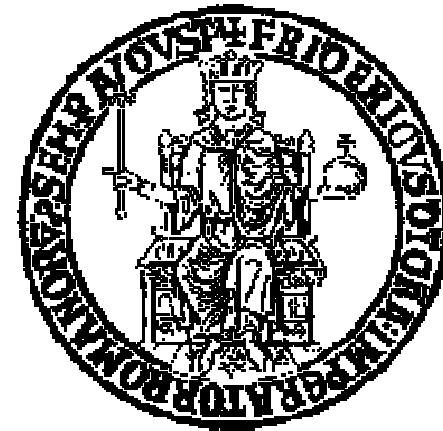
UNIVERSITÀ DEGLI STUDI DI PAVIA

FACOLTÀ DI INGEGNERIA

LABORATORIO DI MICROCALCOLATORI

# Obiettivi

Progetto di Ricerca di Interesse Nazionale



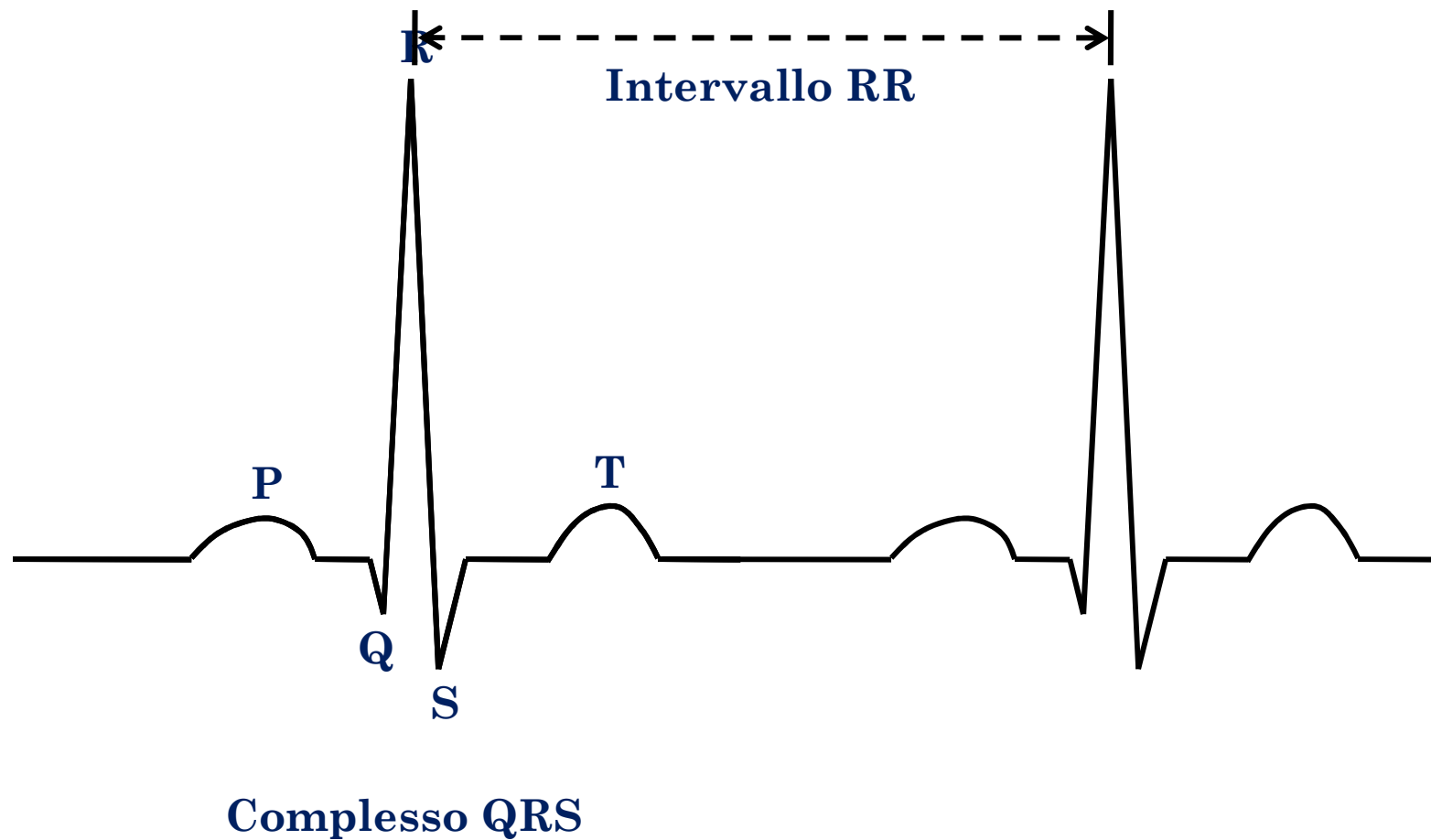
Realizzare un sistema indossabile  
a basso costo e basso consumo  
per misure cardiocografiche fetali in tempo reale

→ embedded

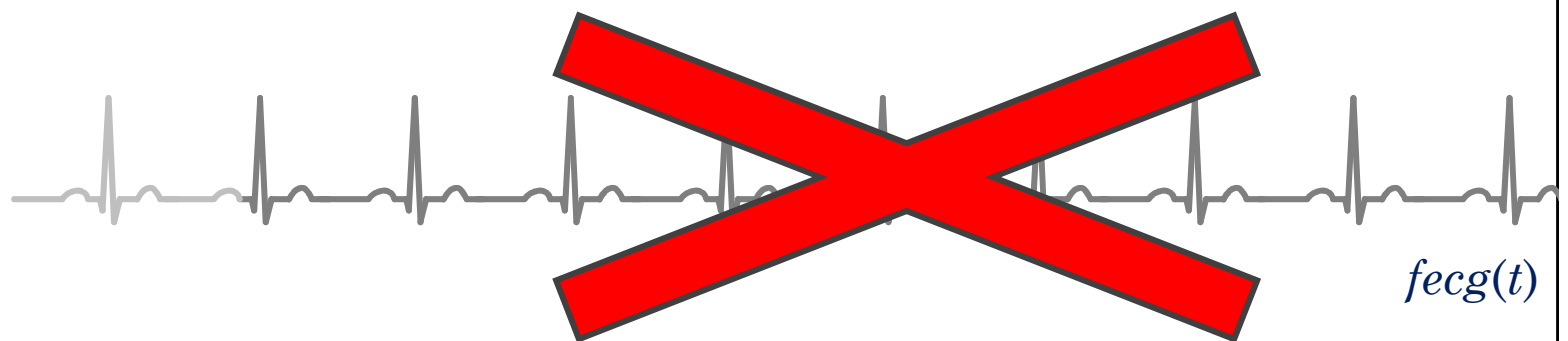
# Sommario

- ECG Fetale
- Algoritmi per la stima del FECG
- Infomax
- Implementazione su FPGA Stratix II
- Conclusioni

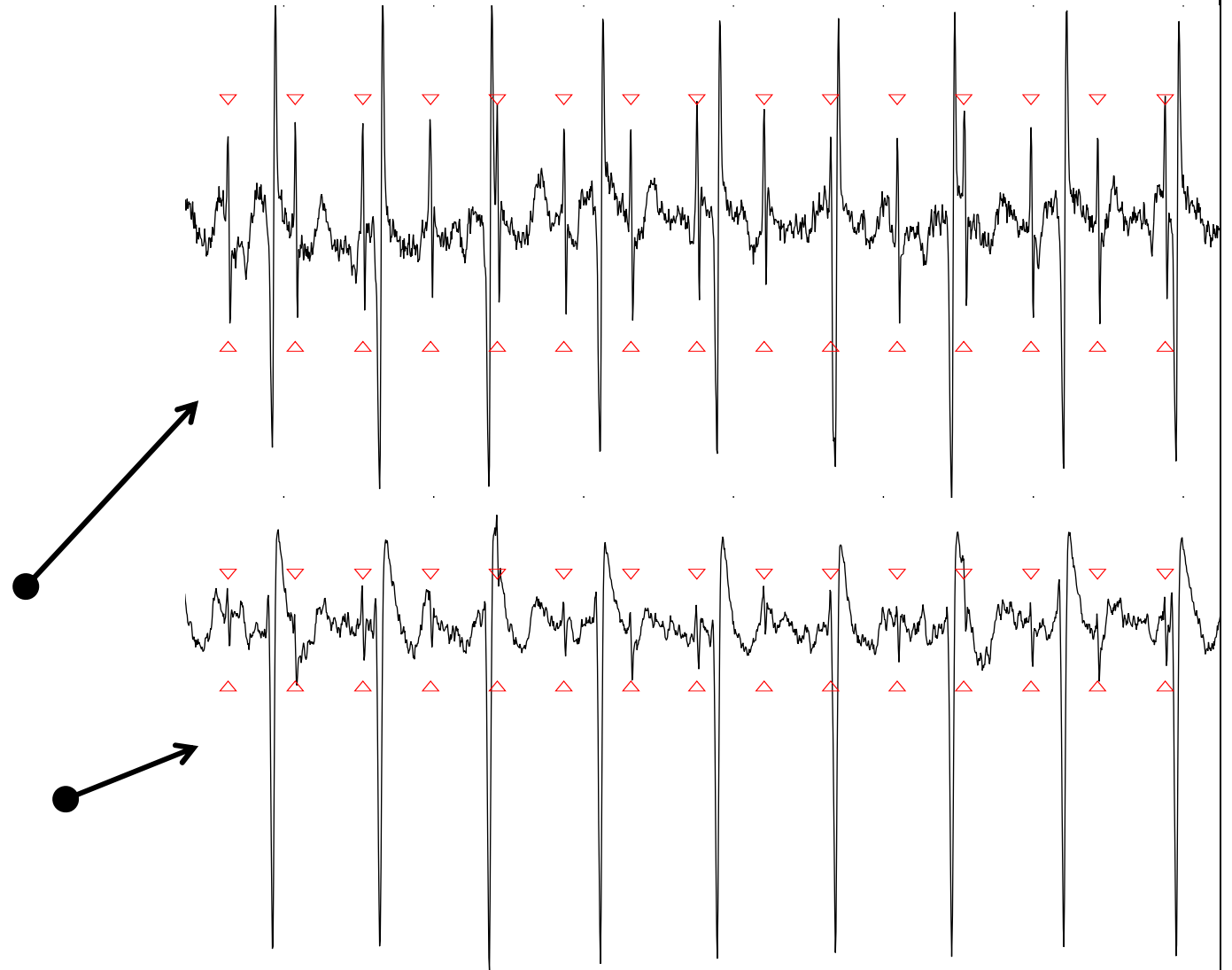
# Frequenza Cardiaca (HR)



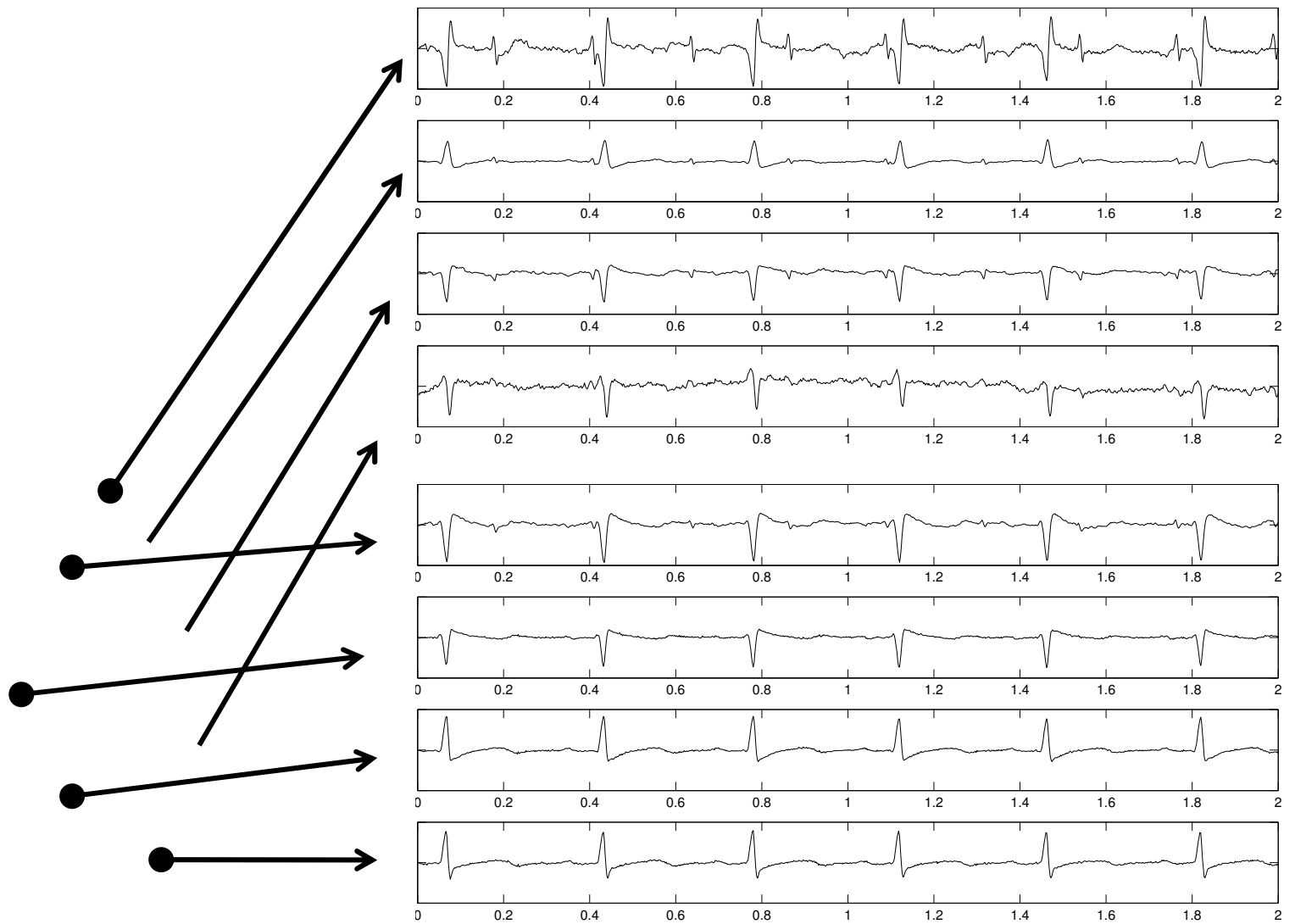
# ECG Fetale (FECG)



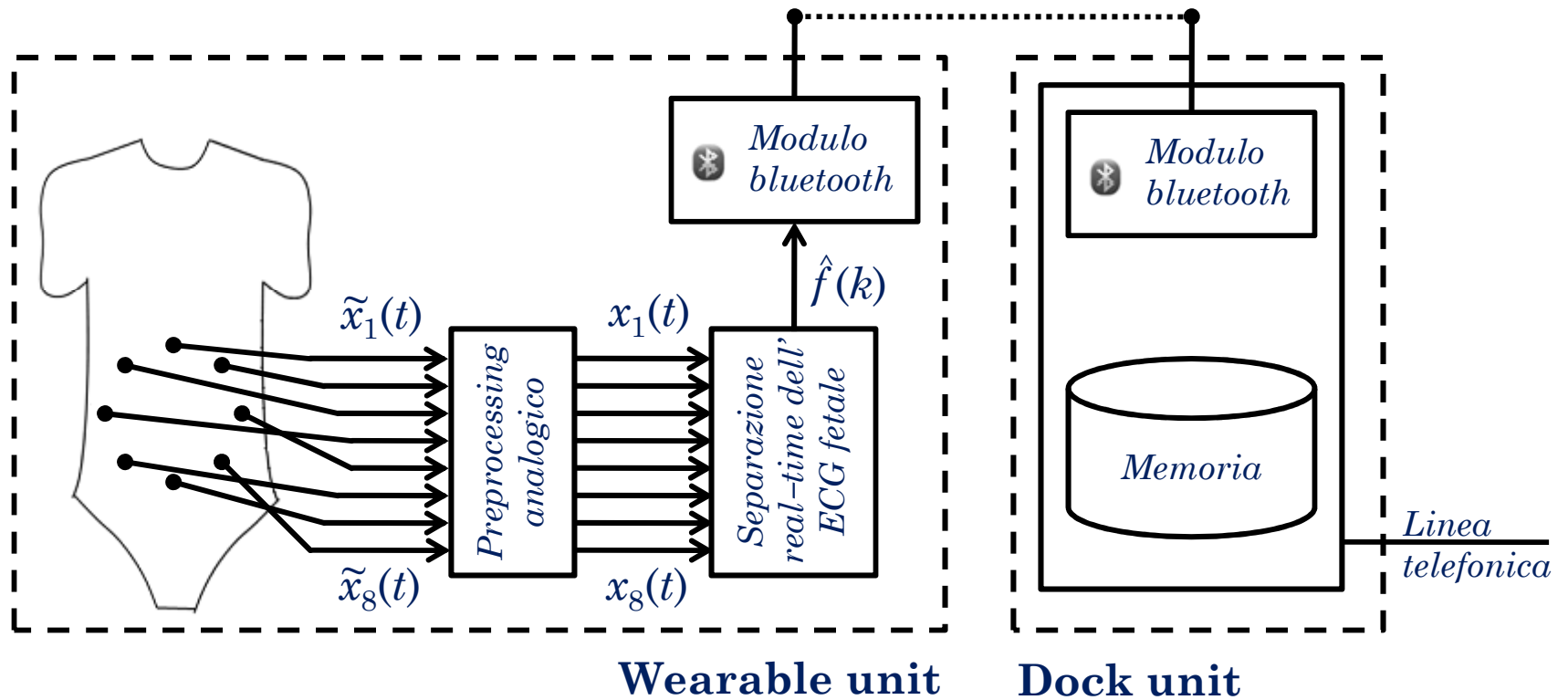
# Misurazioni addominali



# Misurazioni addominali

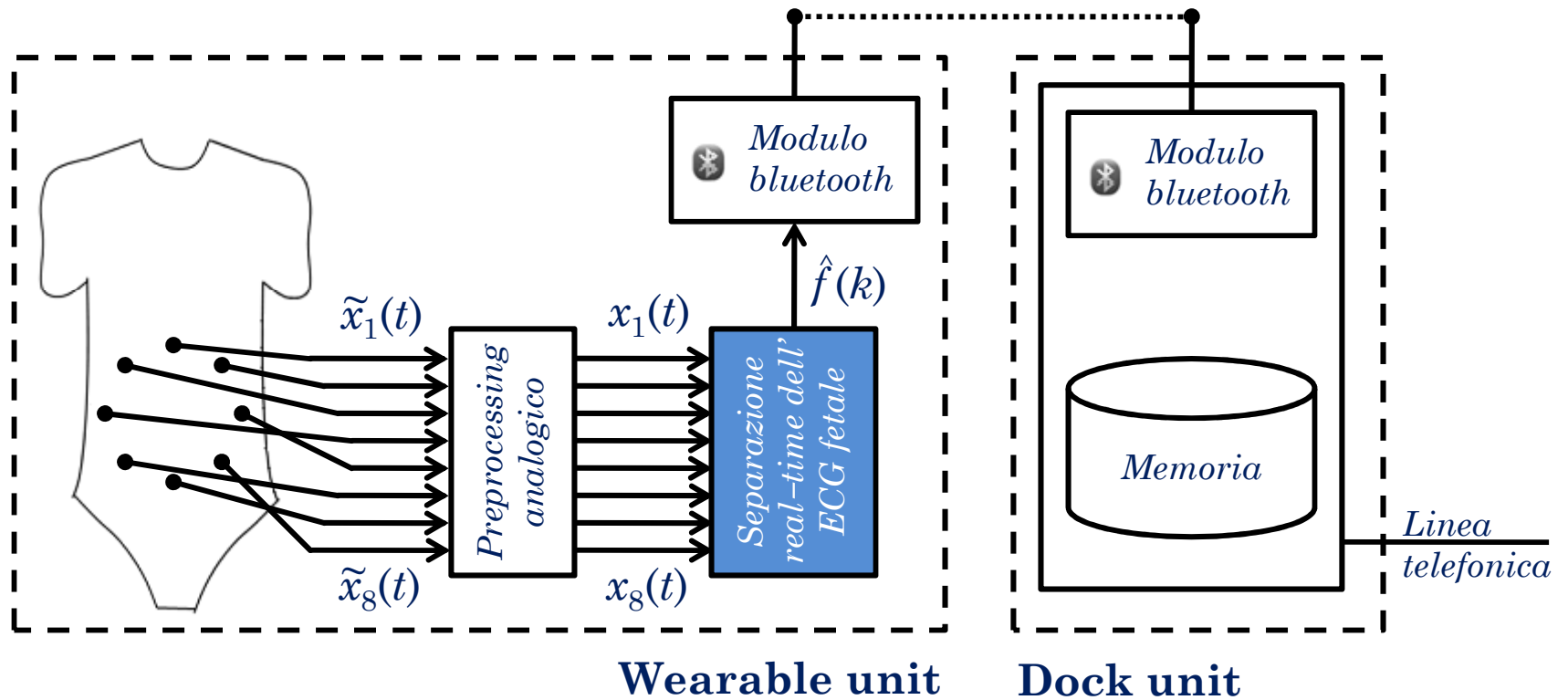


# Sistema proposto





# Sistema proposto



# Algoritmi per la stima del FECG

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# Algoritmi per la stima del FECG

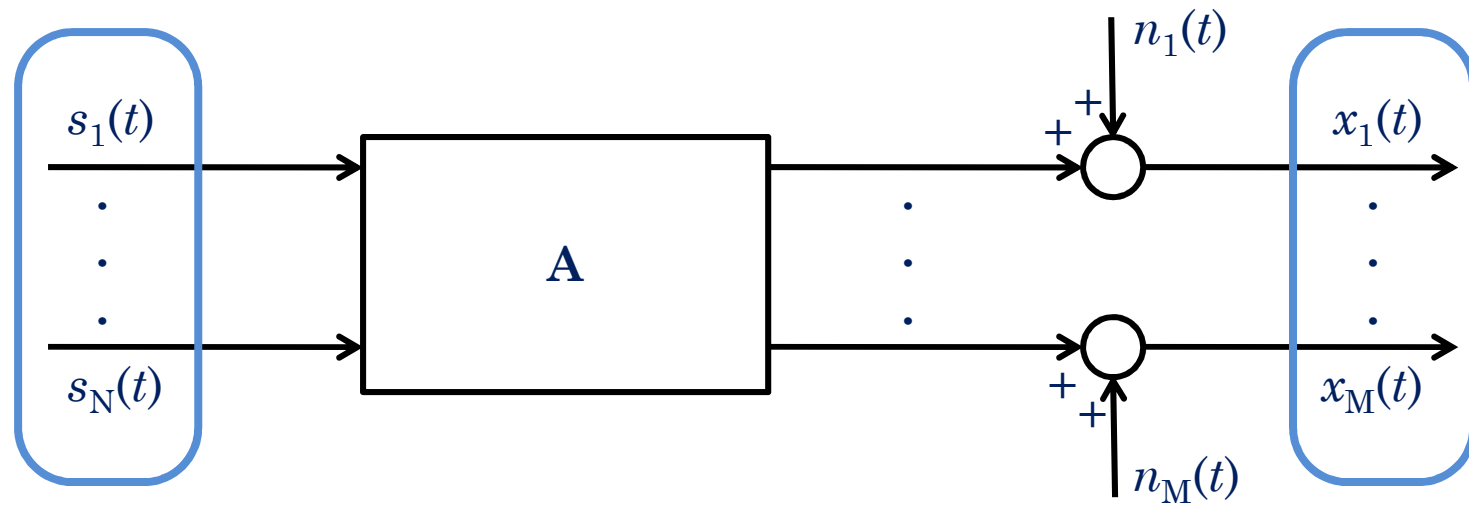
# Infomax

Sviluppato da Bell e Sejnowski nel 1995.

Inizialmente utilizzato per separare mix audio, è stato applicato in vari campi.

Fa parte della famiglia *independent component analysis*.

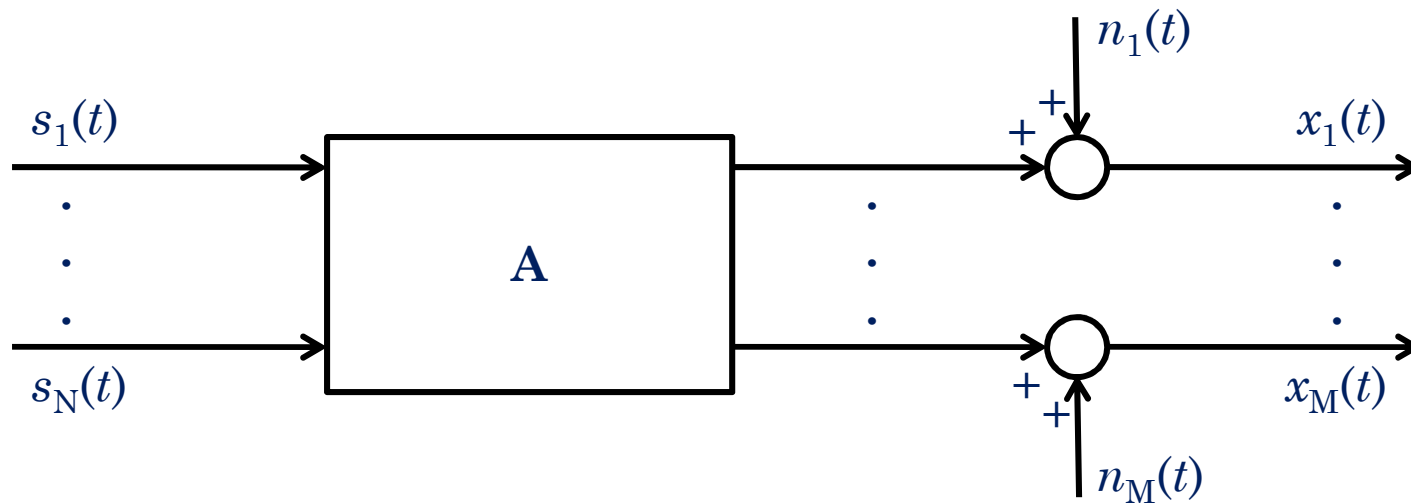
# Modello



- ECG fetale
- ECG materno
- alimentazione di rete
- respiro
- movimento
- rumore di contatto dell'elettrodo
- rumore ambientale

Misure  
addominali

# Modello



$$\mathbf{x}(t) = \mathbf{A}\mathbf{s}(t) + \mathbf{n}(t)$$

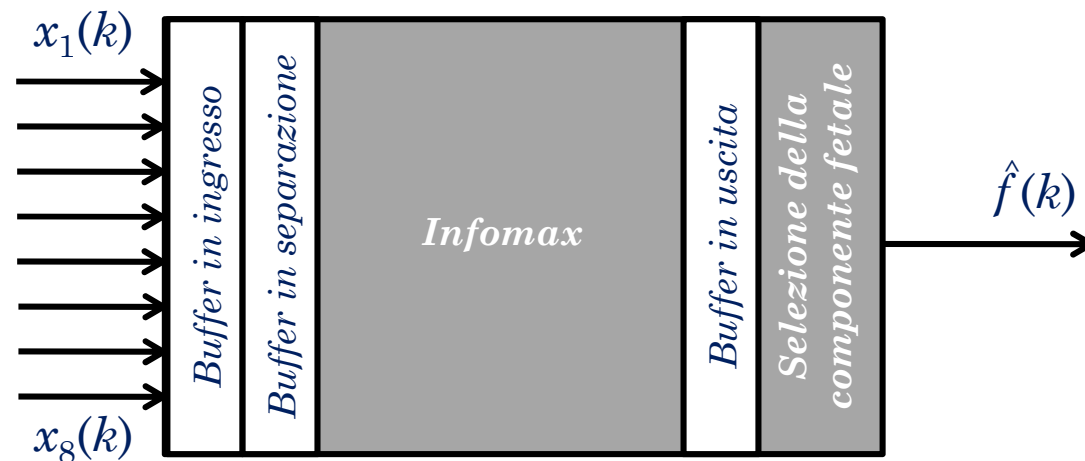
$$\mathbf{s}(t) = \mathbf{A}^{-1}\mathbf{x}(t)$$

$$\hat{\mathbf{s}}(t) = \hat{\mathbf{A}}^{-1}\mathbf{x}(t) = \mathbf{W}(t)$$

approssimazione  
iterativa

# Infomax nell'unità di separazione

Sono necessari alcuni *buffer*, per rendere la separazione *online*.



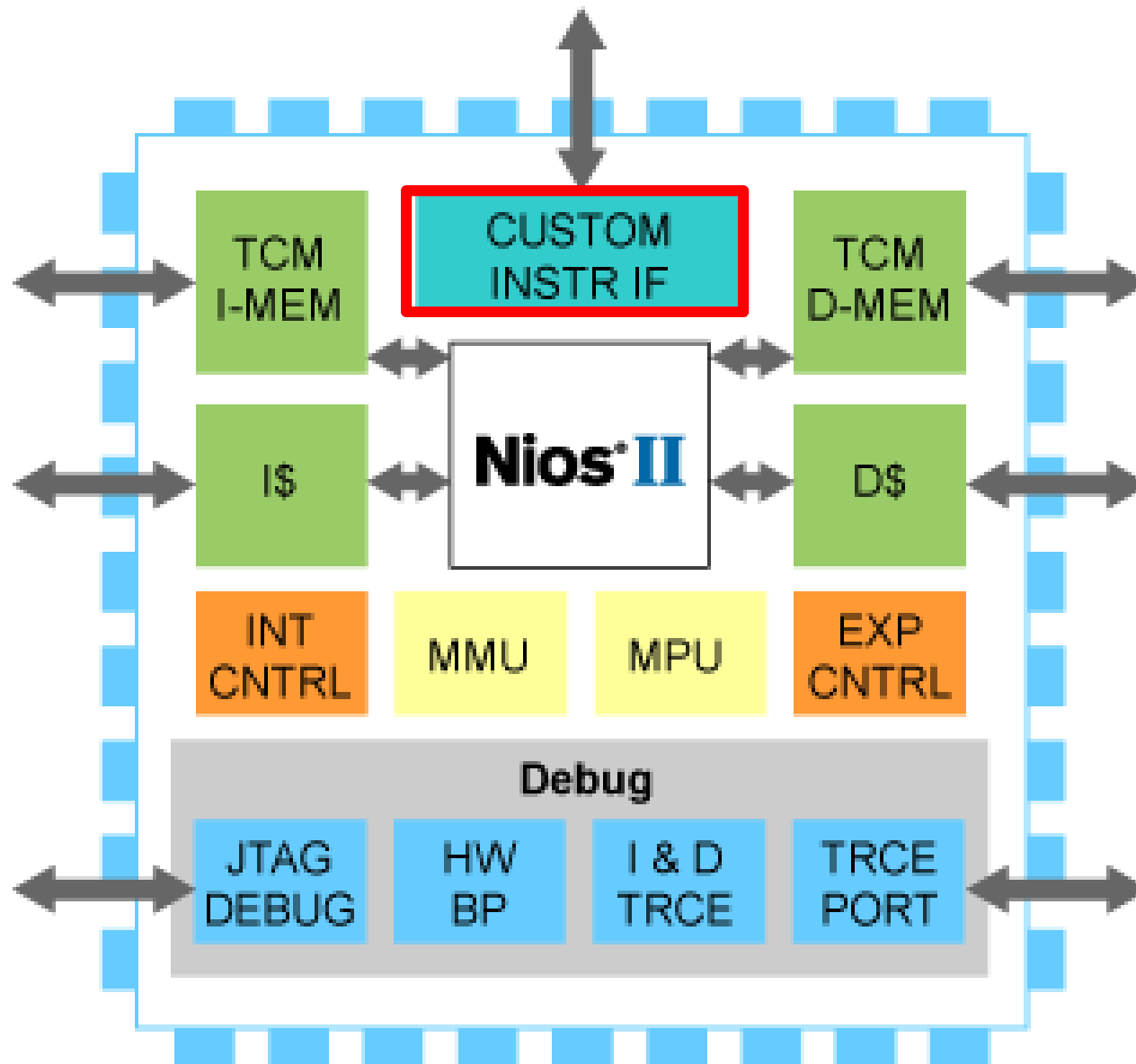
Sono state fatte alcune prove, con il segnale suddiviso in segmenti di 1024 campioni.

# Altera Nios II Development Kit

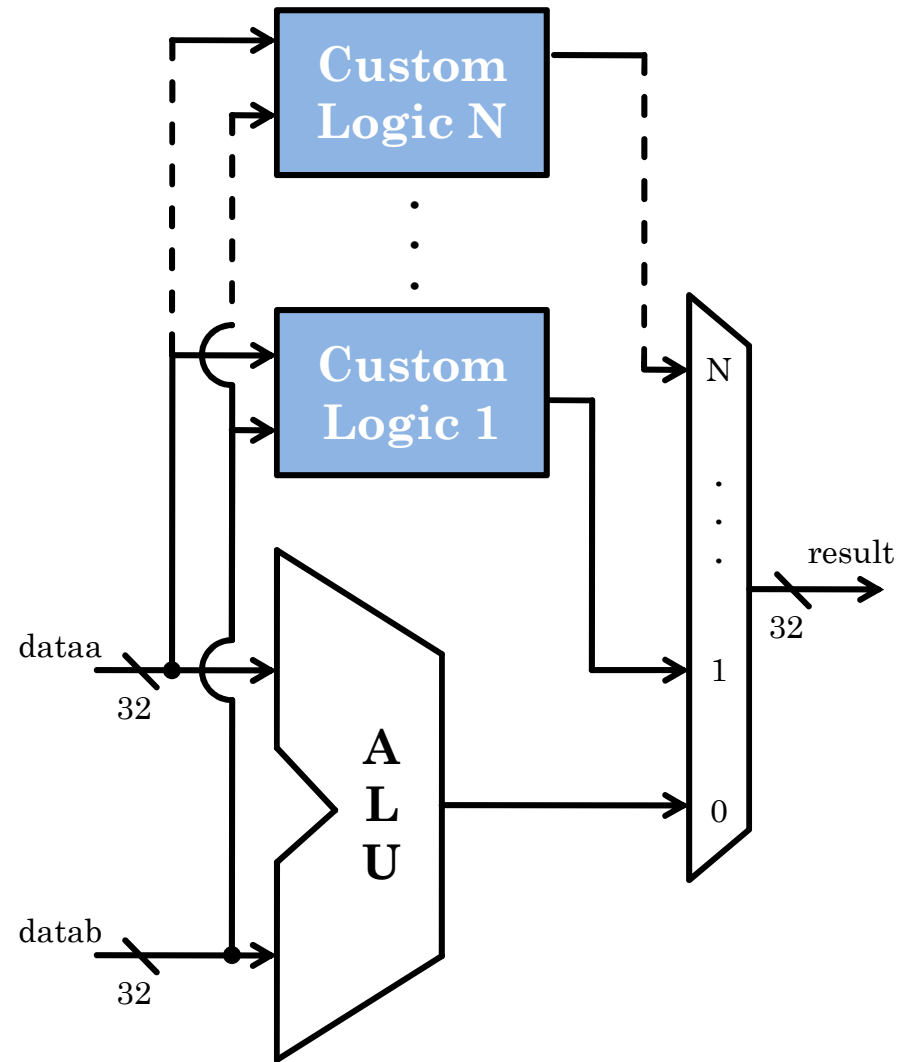
- FPGA Altera Stratix II EP2S60
- 16 MB di memoria Flash;
- 2 MB di memoria sincrona SRAM;
- 32 MB di memoria SDRAM di tipo DDR;
- oscillatore a 50 MHz;
- interfaccia Ethernet;
- *display* a sette segmenti;
- otto *led*;
- quattro pulsanti;
- interfaccia JTAG.



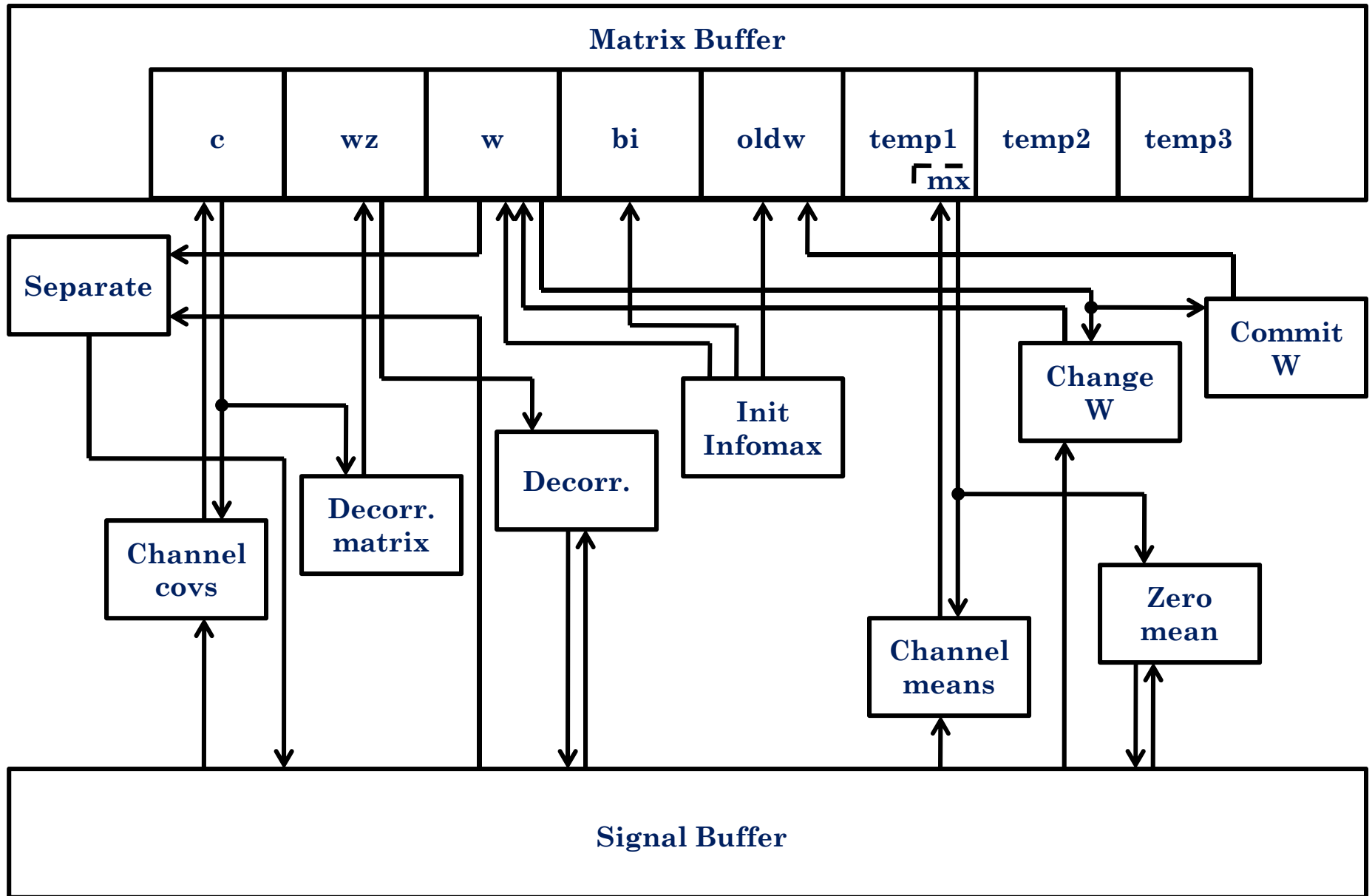
# Custom Instructions



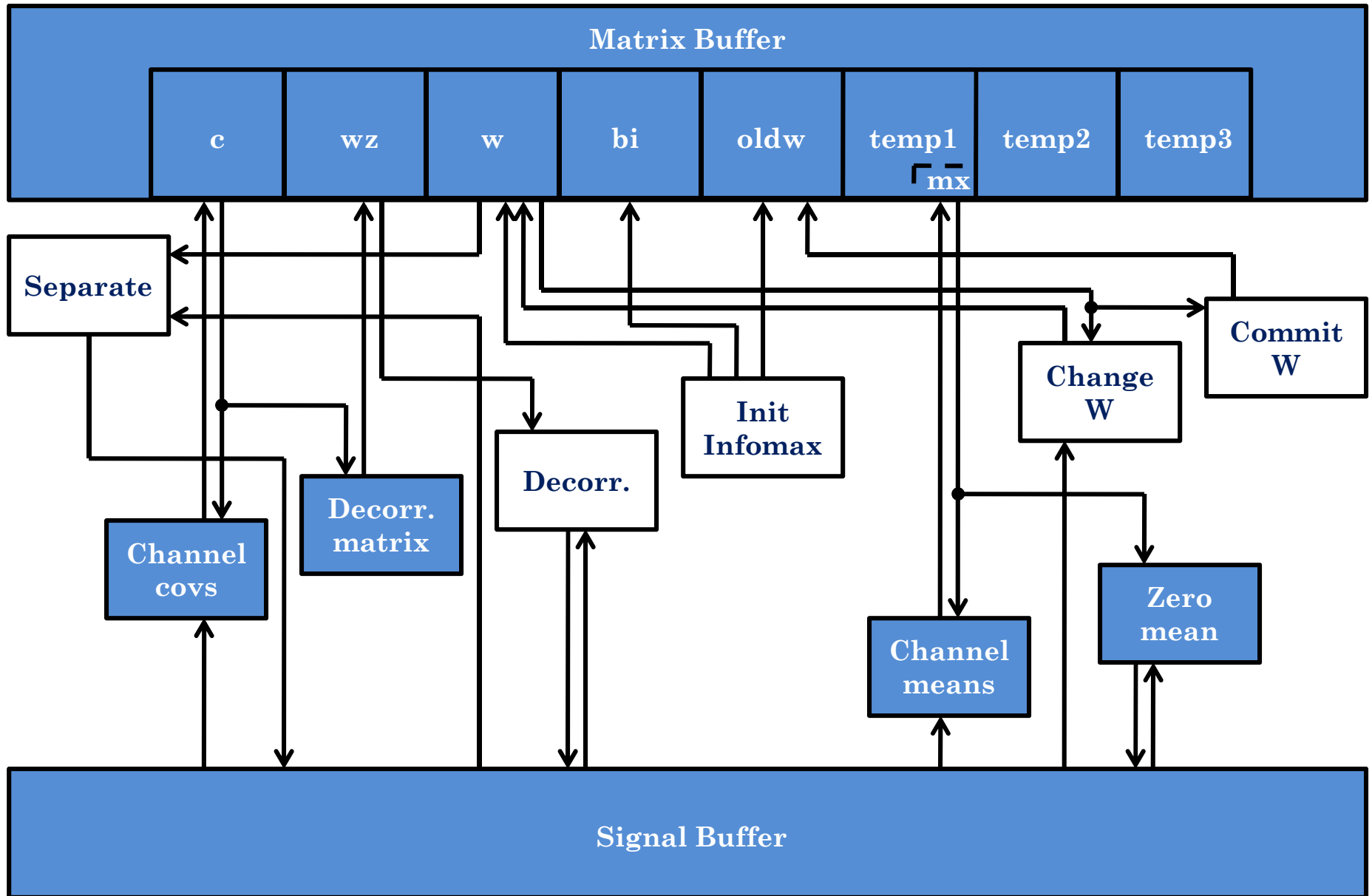
# Custom Instructions



# Infomax su FPGA Stratix II

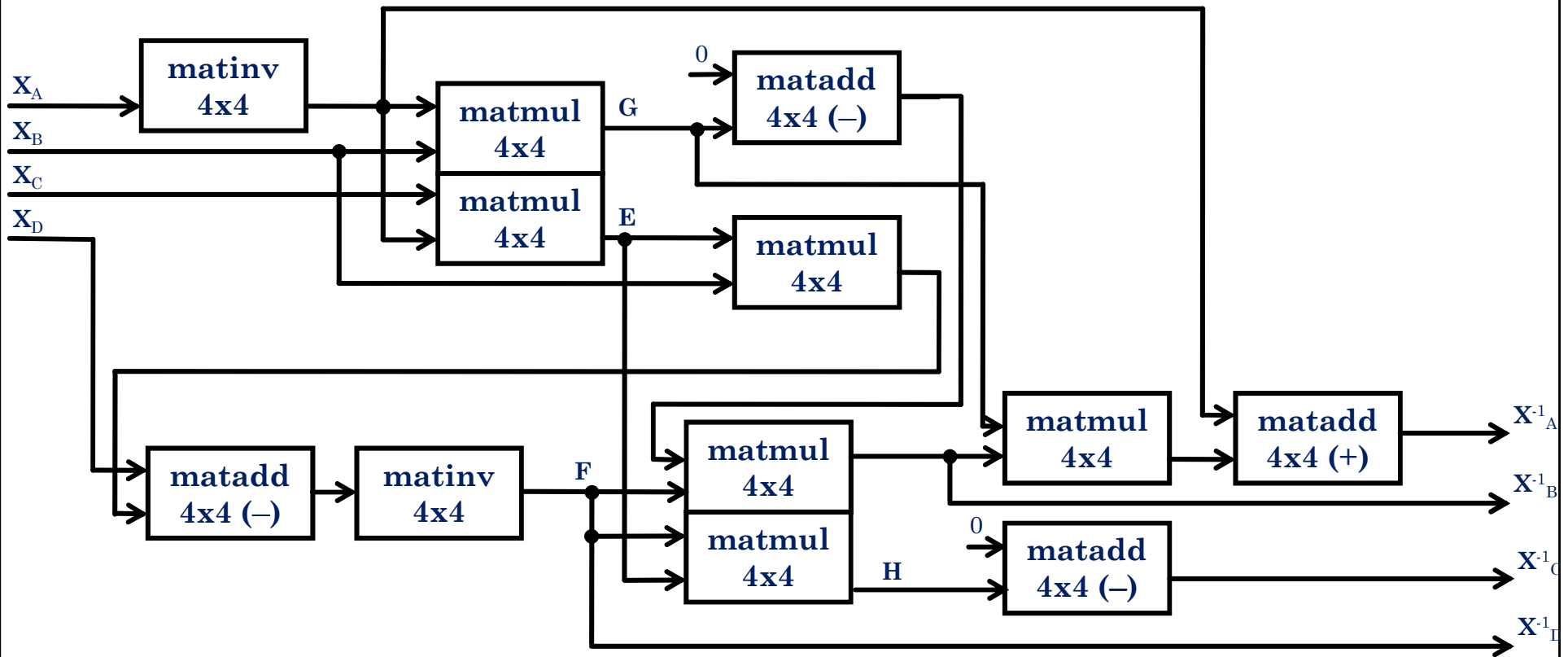


# Infomax su FPGA Stratix II



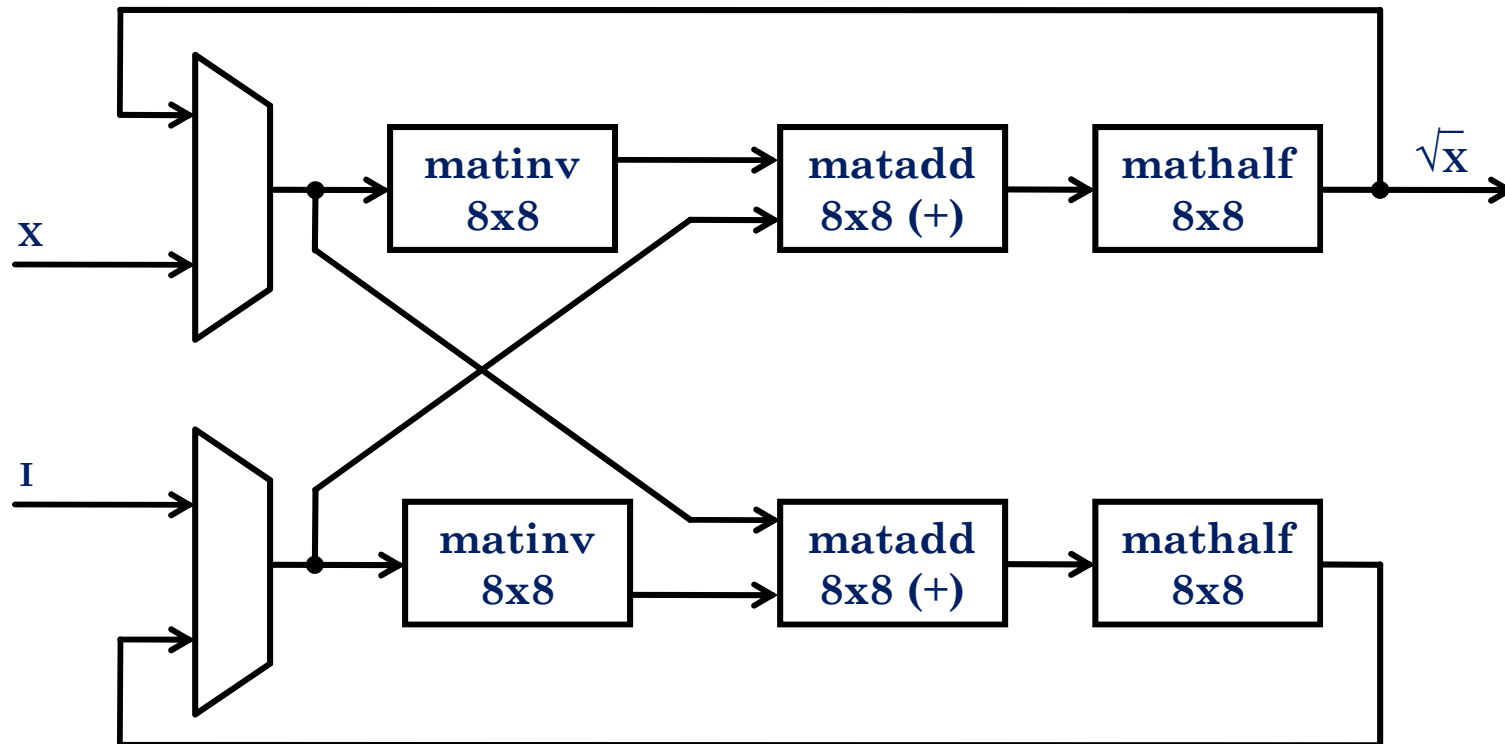
# Infomax su FPGA Stratix II

matinv8x8



# Infomax su FPGA Stratix II

mat\_sqrt8x8



# Risultati su FPGA Stratix II



8.54  
ms

<<

652  
ms

Tempo di esecuzione  
totale di quanto  
sviluppato su FPGA.

(50MHz)

Tempo di esecuzione  
della stessa parte su  
ARM 9.

(400MHz)

# Conclusioni

È stato individuato un algoritmo efficace per la separazione del FECG.

È stata progettata una soluzione FPGA.

Di questa è stata sviluppata una parte, nettamente migliore in termini di efficienza rispetto all'equivalente implementazione software.





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