



# Innovate Italy

## Altera Design Contest 2012

### Submission and Evaluation Guidelines

#### **Submission Deadline:**

- Team Proposal Submission Deadline: **October 31, 2012**
- Detailed Project Progress Paper Submission Deadline: **March 15, 2013**
- Final Project Submission Deadline: **March 15, 2013**

**Deliverables:** Design Contest participants are required to submit the following:

- Each individual participant in this contest will be required to sign Innovate Italy 2012 Contest Participant Release Form.
- Preliminary Paper and Final Project Paper should be submitted before the deadline.
- Compilation report file and simulation waveforms showing correct functionality of the design. Altera may ask for more details on the design such as RTL simulation results etc if required.
- In-system demonstrations of the design that shows correct hardware functionality of the designs. Experts from Altera and Terasic will oversee the final project paper and demonstrations.

#### **Important Notice:**

- Detailed Project Progress Paper and Final Project Paper should accord with the template specified online. [The Project Paper Submission Template](#) and [Innovate Italy 2012 Contest Participant Release Form](#) could be referred on **Design Resources** of the website.

- Participants will receive ID number for logging into [www.innovateitaly.com](http://www.innovateitaly.com) to submit/edit their preliminary and final papers.
- By signing Innovate Italy 2012 Contest Participant Release Form, you certify that the project papers and supporting materials you submit and display during this contest are your original work and that you are not infringing any third party intellectual property rights. By signing this release form, you will also transfer the copyright ownership of your project papers and supporting materials to Altera. You and the other members of your project team will retain the right to reproduce, distribute, and create derivative works of your project papers and all supporting materials.
- Altera, as the sponsor of this contest, will retain the copyright ownership of the project papers and other usufruct of the design and documents of this contest.

**Evaluation Methodology:**

1. The designs will be scored by a panel of experts from Altera, and Terasic.
2. The score will be calculated based on the scoring guidelines mentioned in Table 1
3. The design receiving the highest score will be declared the 1<sup>st</sup> prize winner. There will also be one 2<sup>nd</sup> and one 3<sup>rd</sup> prize for the designs receiving the 2<sup>nd</sup> highest and the 3<sup>rd</sup> highest scores.

**Table 1: Scoring Guidelines for Innovate Italy-Altera Design Contest 2012**

| <b>Design Phase</b>   | <b>Category</b>   | <b>Score</b>         | <b>Examples</b>                                                                             |
|-----------------------|-------------------|----------------------|---------------------------------------------------------------------------------------------|
| <b>Design Concept</b> | <b>Complexity</b> | 5 pts                | -Design uses RTOS<br>or<br>-Multiple Nios cores sharing and inter-core communications       |
|                       |                   | 4 pts                | - Uses DSP Algorithm<br>or<br>- Does packet processing<br>or<br>- Does graphic acceleration |
|                       |                   | 3 pts                | - greater than 70% LE /memory utilization<br>or<br>- uses complex IP cores                  |
|                       |                   | 2 pts                | - uses two masters on Avalon bus                                                            |
|                       |                   | 1 pts                | - greater than 50% LE / memory utilization                                                  |
|                       |                   | 0 pt                 | - None of the above                                                                         |
|                       |                   | <b>Functionality</b> | 5 pts                                                                                       |
|                       | 4 pts             |                      | - custom instruction<br>or<br>- custom peripheral for hardware acceleration                 |
|                       | 3 pts             |                      | - custom peripheral without hardware acceleration                                           |
|                       | 2 pts             |                      | - More than 8 peripherals on SoPC bus                                                       |
|                       | 1 pts             |                      | - More than 5 peripherals on SoPC bus                                                       |
|                       | 0 pts             |                      | - None of the above                                                                         |

|                                   |                     |       |                                                                                                                             |
|-----------------------------------|---------------------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| <b>Design Implementation</b>      | <b>Completeness</b> | 5 pts | - Final report and 100% software complete and 100% hardware demonstration                                                   |
|                                   |                     | 4 pts | - Final report and 100% software and 80% hardware demonstration                                                             |
|                                   |                     | 3 pts | - Final report and software debugging AND hardware debugging                                                                |
|                                   |                     | 2 pts | - Final report and software debugging                                                                                       |
|                                   |                     | 1 pts | - Final report and hardware debugging only                                                                                  |
|                                   |                     | 0 pts | - None of the above                                                                                                         |
| <b>Documentation Completeness</b> | <b>Completeness</b> | 5 pts | - Complete all 7 parts in proper format with proper illustrations and full documentation of the final project.              |
|                                   |                     | 4 pts | - Complete all 7 parts in proper format                                                                                     |
|                                   |                     | 3 pts | - Complete mandatory parts and detailed design description and design features                                              |
|                                   |                     | 2 pts | - Complete mandatory parts and detailed design description                                                                  |
|                                   |                     | 1 pts | - Complete all mandatory parts (Design Introduction, Function Description, Performance Parameters, and Design Architecture. |
|                                   |                     | 0 pts | - No submission *<br>*Violation of the contest agreements. The project is said to be disqualified.                          |