**Innovate Italy**

**Altera Design Contest 2012**

**Project Paper Submission Template**

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| **Importance Notice** | 1) **Submission Deadline**<br>I) Team Proposal Submission Deadline **October 31, 2012**<br>II) Detailed Project Progress Submission Deadline: **March 15, 2013**<br>II) Final Project Paper Submission Deadline: **March 15, 2013**<br>*Please log in www.innovateitaly.com with your ID number and Submit the paper before the deadline.<br><br>2) **Deliverables**: Design Contest participants are required to submit:<br>I) Team Proposal- Complete **Part I** before **October 31, 2012**<br>II) Detailed Project Progress- **Part I ~ Part VII**<br>II) Final Project Paper - **All sections should be completed**<br><br>3) Altera, the sponsor of the contest, holds the copyright and the usufruct of all the designs and their documents of this contest.<br><br>4) Each team member should sign and return **Innovate Italy 2012 Contest Participant Release Form** |

**PART I Design Introduction**

Please give some general information of your design, e.g. purpose of the design, application scope, and targeted users. Please also include a detailed description of why you used Altera FPGA devices to do the design.

**PART II** Function Description

Please give detailed information to show the functionality of your design and how to implement it.

**PART III** Performance Parameters
Please enumerate some performance parameters that the design needs to reach.
If possible, please compare the actual performance realized in your design with the design parameter, and then appraise the function of Altera FPGA devices in the design.

**PART IV** Design Architecture
Please give the system design scheme of your design or both hardware design block diagram and software flow chart.

**PART V** Design Methodology
Please give the detailed description of the implementation method and steps of the design, especially how the design is implemented using the concept of SOPC.

**PART VI** Design Features
Please enumerate the outstanding features of your design and what aspects of Nios helped you to implement them.

**PART VII** Conclusion
What you learned during the design? During this contest, you certainly increased your understanding of Altera FPGA devices and made some conclusions. These conclusions will be useful for others who are learning about Altera FPGA devices or using Altera FPGA devices as reference. Please tell us what you learned during the design.